100GE/OTU4 CFP4 SR4 100m Optical Transceiver

P/N: GF4-M101-SR4C

Features

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 28Gbps per channel
- 4 channels 850nm VCSEL array
- 4 channels PIN photo-detector array
- Low power consumption < 2.5W
- Up to 28Gb/s data rate per channel
- Hot-pluggable CFP4 form-factor
- Maximum link length of 70m on OM3 Multimode Fiber (MMF) and 100m on OM4 MMF
- Single MPO connector receptacle
- MDIO management interface
- Operating case temperature range: 0°C to +70°C
- 3.3V power supply voltage
- RoHS-6 compliant (lead free)

Applications

- IEEE 802.3bm 100GBASE-SR4
- OTN OTU4
- 128G (4x32G) Fibre Channel

Description

The Gigalight 100GE/OTU4 CFP4 SR4 100m optical transceiver (GF4-M101-SR4C) is a hot-pluggable module designed for optical communication applications compliant to the IEEE 802.3bm 100GBASE-SR4, OTN OTU4, and 128G (4x32G) Fibre Channel standards. The module converts 4 input channels of 28Gb/s electrical data to 4 channels of VCSEL optical signals over 4 multimode fibers for 112Gb/s optical transmission. Reversely, on the receiver side, the module receives 4 channels of VCSEL optical signals over 4 multimode fibers and then converts them to 4 output channels of electrical data.

The high-speed VCSEL transmitters and high-sensitivity PIN receivers provide superior performance for 100G applications up to 100m links over OM4 multimode fibers and compliant to optical interface with IEEE

802.3bm Clause 95 100GBASE-SR4 requirements.

This product contains an MTP/MPO optical connector for the optical interface and a 56-pin connector for the electrical interface. Figure 1 shows the functional block diagram of this product.

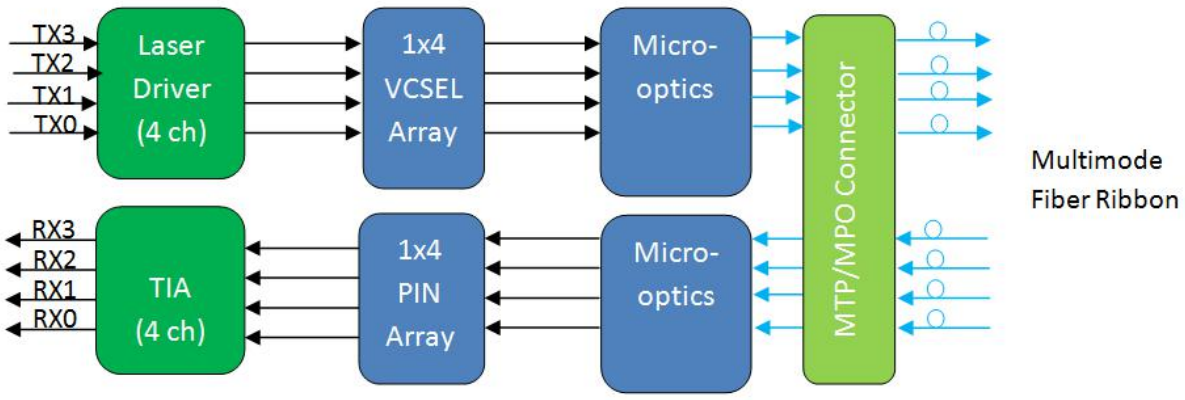

Figure 1. 100G CFP4 SR4 Transceiver Block Diagram

MDIO Interface

The CFP4 module supports the MDIO interface specified in IEEE 802.3bm Clause 45. It supportsalarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6 wires including 2 wires of MDC and MDIO, as well as 3 Port Address wires, and the Global Alarm wire. The CFP4 uses pins in the electrical connector to instantiate the MDIO interface as listed in Table 1. MDIO Interface Pins.

Table 1. MDIO Interface Pins

PIN	Symbol	Description	I/O	Logic	"H"	"L"
13	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS		
17	MDC	MDIO Clock	I	1.2V LVCMOS		
19	PRTADR0	MDIO port address bit 0	I	1.2V LVCMOS	per MDIO document	
20	PRTADR1	MDIO port address bit 1	I	1.2V LVCMOS		
21	PRTADR2	MDIO port address bit 2	I	1.2V LVCMOS		

Pin Assignment and Description

The CFP4electrical connector has 56 pins, which are arranged in top and bottom rows. The pin orientation is shown in Figure 2 and the pin map is shown in Table 2. The detailed description of the bottom side pins from pin 1 through pin 28 is shown in Table 3 while the description of the top side pins is shown in Table 4.

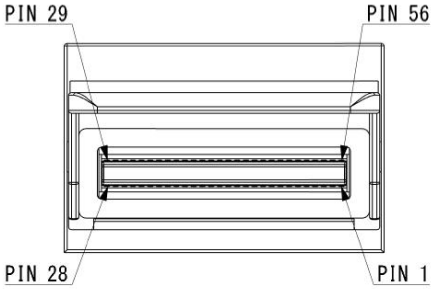

Figure 2. CFP4 Connector Pin Map Orientation

Table 2. Pin Map

	CFP4 Bottom		CFP4 Top	CFP4 Top ALT1	
1	3.3V_GND	56	GND	GND	
2	3.3V_GND	55	TX3n	TX0n	
3	3.3V	54	TX3p	TX0p	
4	3.3V	53	GND	GND	
5	3.3V	52	TX2n	TX1n	
6	3.3V	51	TX2p	TX1p	
7	3.3V_GND	50	GND	GND	
8	3.3V_GND	49	TX1n	TX2n	
9	VND_IO_A	48	TX1p	TX2p	
10	VND_IO_B	47	GND	GND	
11	TX_DIS *(PRG_CNTL1)*	46	TX0n	TX3n	
12	RX_LOS *(PRG_ALRM1)*	45	TX0p	TX3p	
13	GLB_ALRMn	44	GND	GND	
14	MOD_LOPWR	43	*(REFCLKn)*	*(REFCLKn)*	REFCLK (Optional)
15	MOD_ABS	42	*(REFCLKp)*	*(REFCLKp)*	
16	MOD_RSTn	41	GND	GND	
17	MDC	40	RX3n	RX3p	
18	MDIO	39	RX3p	RX3n	
19	PRTADR0	38	GND	GND	
20	PRTADR1	37	RX2n	RX2p	
21	PRTADR2	36	RX2p	RX2n	
22	VND_IO_C	35	GND	GND	
23	VND_IO_D	34	RX1n	RX1p	
24	VND_IO_E	33	RX1p	RX1n	
25	GND	32	GND	GND	
26	*(MCLKn)*	31	RX0n	RX0p	MCLK = TX_MCLK + RX_MCLK (Optional)
27	*(MCLKp)*	30	RX0p	RX0n	
28	GND	29	GND	GND	

Table 3. Definition of the Bottom Side Pins from Pin 1 through Pin 28

PIN	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground
2	3.3V_GND			GND
3	3.3V			3.3V Module Supply Voltage
4	3.3V			3.3V Module Supply Voltage
5	3.3V			3.3V Module Supply Voltage
6	3.3V			3.3V Module Supply Voltage
7	3.3V_GND			GND
8	3.3V_GND			GND
9	VIND_IO_A	I/O		Module Vendor I/O A. Do Not Connect
10	VIND_IO_B	I/O		Module Vendor I/O B. Do Not Connect
11	TX_DIS (PRG_CNTL1)	I	LVCMOS w/PUR	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled.(Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS (PRG_ALRM1)	O	LVCMOS w/PUR	Receiver Loss of Optical Signal. "1": low optical signal; "0":normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVCMOS	Global Alarm. "0":alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host
14	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0":power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host
16	MOD_RSTn	I	LVCMOS w/PDR	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data(electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect

24	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect
25	GND			GND
26	(MCLKn)	O	CML	For optical waveform testing. Not for normal use
27	(MCLKp)	O	CML	For optical waveform testing. Not for normal use
28	GND			GND

Table 4. Definition of Top Side Pins

PIN	Name		PIN	Name
29	GND		43	(REFCLKp)
30	RX0p		44	GND
31	RX0n		45	TX0p
32	GND		46	TX0n
33	RX1p		47	GND
34	RX1n		48	TX1p
35	GND		49	TX1n
36	RX2p		50	GND
37	RX2n		51	TX2p
38	GND		52	TX2n
39	RX3p		53	GND
40	RX3n		54	TX3p
41	GND		55	TX3n
42	(REFCLKn)		56	GND

Optical Interface Lanes and Assignment

Figure 3 shows the orientation of the multi-mode fiber facets of the optical connector. Table 5 provides the lane assignment.

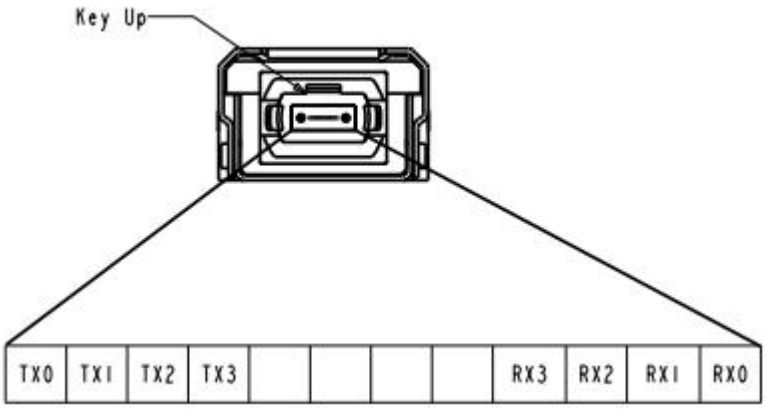

Figure 3.Outside View of the CFP4 Module MPO Receptacle

Table5: Lane Assignment

Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5,6,7,8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	Ts	-40	85	degC	
Relative Humidity (non-condensation)	RH		85	%	
Operating Case Temperature	T_{OP}	0	70	degC	
Supply Voltage	Vcc	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.3	V	
LVTTL Output Current	Iolvttl		15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Damage Threshold, each Lane	TH_d	3.4		dBm	1

Notes:

1. PIN receiver.

Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	

Data Rate, each Lane			25.78125		Gbps	1
Data Rate, each Lane			27.9525		Gbps	2
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Power Supply Noise	Vrip			2	%	DC-1MHz
				3	%	1-10MHz
Link Distance (OM3 MMF)	D1			70	m	
Link Distance (OM4 MMF)	D2			100	m	

Notes:

1. 100GBASE-SR4.
2. OUT4 with FEC.

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Power Consumption				2.5	W	
Supply Current	Icc			800	mA	
Low Power Mode Power Dissipation				1	W	
Transmitter (each Lane)						
Single-ended Input Voltage Tolerance (Note 1)		-0.3		4.0	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Receiver (each Lane)						

Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	

Notes:

1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Center Wavelength	λ_C	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda_{rms}$			0.6	nm	
Average Launch Power, each Lane	P_{AVG}	-8.4		2.4	dBm	
Optical Modulation Amplitude (OMA), each Lane	P_{OMA}	-6.4		3.0	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			4.0	dB	
Launch Power in OMA minus TDEC, each Lane		-7.3			dBm	
Transmitter and Dispersion Eye Closure (TDEC), each Lane				4.3	dB	
Extinction Ratio	ER	2.0			dB	
Optical Return Loss Tolerance	TOL			12	dB	
Encircled Flux		≥86% at 19um ≤ 30% at 4.5um				
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}, 5×10^{-5}		{0.3,0.38,0.45,0.35,0.41,0.5 }				2

hits/sample						
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Receiver						
Center Wavelength	λ_C	840	850	860	nm	
Damage Threshold, each Lane	TH_d	3.4			dBm	3
Average Receive Power, each Lane		-10.3		2.4	dBm	
Receiver Reflectance	R_R			-12	dB	
Receive Power (OMA), each Lane				3.0	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-5.2	dBm	4
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5	2		dB	
Conditions of Stress Receiver Sensitivity Test (Note 5):						
Stressed Eye Closure (SEC), Lane under Test			4.3		dB	
Stressed Eye J2 Jitter, Lane under Test			0.39		UI	
Stressed Eye J4 Jitter, Lane under Test				0.53	UI	
OMA of each Aggressor Lane			3		dBm	
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.28,0.5,0.5,0.33,0.33,0.4}				

Notes:

1. Even if the TDP < 0.9 dB, the OMA minmust exceed the minimum value specified here.
2. See Figure 5 below.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
5. Stressed eye closure and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

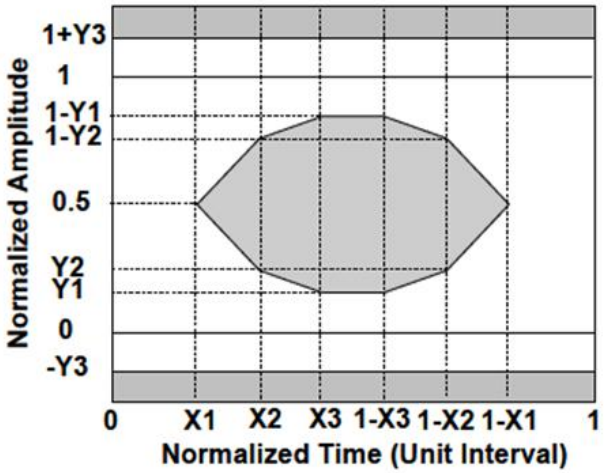

Figure 5.Eye Mask Definition

Digital Diagnostic Functions (Optional)

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified. It is compliant to SFF-8436.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.15	0.15	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	Ch1~Ch4
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/-3 dB total accuracy.

Mechanical Dimensions

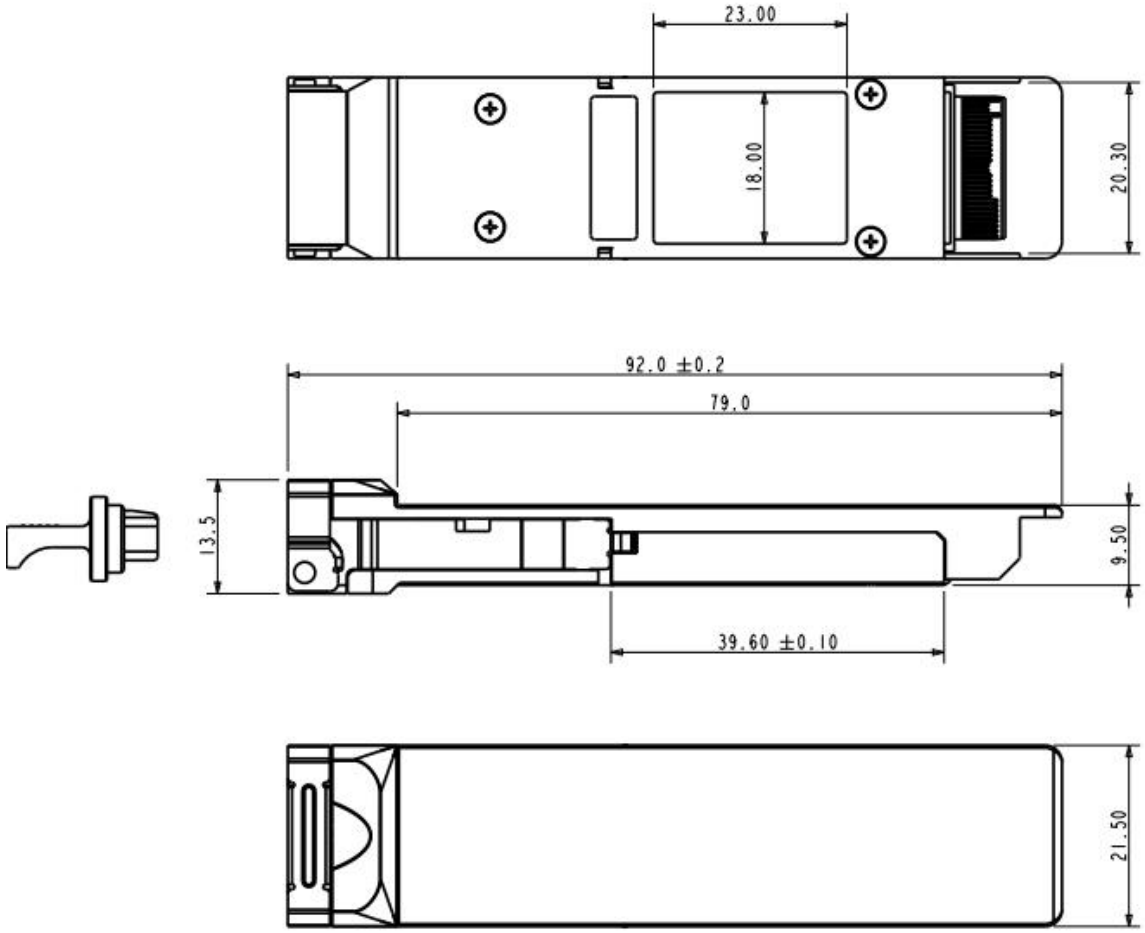

Figure 6.Mechanical Outline

ESD

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Part Number Ordering Information

GF4-M101-SR4C	100GE/OTU4 CFP4 SR4, 112Gb/s, up to reach 70m on OM3 MMF and 100m on OM4 MMF

Important Notice

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